

LQFP176	Pin Name	Pad type	IO Pull	Reset State	Default function	Defual function description	Function 2
1	DDR_A0	A			DDR_A0	DDR3 PHY	
2	DDR_A2	A			DDR_A2	DDR3 PHY	
3	DDR_A5	A			DDR_A5	DDR3 PHY	
4	DDR_A9	A			DDR_A9	DDR3 PHY	
5	DDR_A13	A			DDR_A13	DDR3 PHY	
6	DDR_A7	A			DDR_A7	DDR3 PHY	
7	DDR_ODT1	A			DDR_ODT1	DDR3 PHY	
8	DDR_DQ10	A			DDR_DQ10	DDR3 PHY	
9	DDR_DQ8	A			DDR_DQ8	DDR3 PHY	
10	VCC_DDR1	P			VCC_DDR1	DDR3 PHY IO Power 1.5V	
11	DDR_DQS1	A			DDR_DQS1	DDR3 PHY	
12	DDR_DQS1_N	A			DDR_DQS1_N	DDR3 PHY	
13	CVDD1	P			CVDD1	DDR3 PHY CORE Power	
14	DDR_DQ14	A			DDR_DQ14	DDR3 PHY	
15	DDR_DQ12	A			DDR_DQ12	DDR3 PHY	
16	DDR_DQ15	A			DDR_DQ15	DDR3 PHY	
17	DDR_DQ13	A			DDR_DQ13	DDR3 PHY	
18	VCC_DDR2	P			VCC_DDR2	DDR3 PHY IO Power 1.5V	
19	DDR_DQ9	A			DDR_DQ9	DDR3 PHY	
20	DDR_DM1	A			DDR_DM1	DDR3 PHY	
21	DDR_DQ11	A			DDR_DQ11	DDR3 PHY	
22	PLL_VCC33	P			PLL_VCC33	DPLL/APLL/GPLL_VCC33	
23	PLL_DVDD11	P			PLL_DVDD11	DPLL/APLL/GPLL_CORE11	
24	VCCIO1	P			VCCIO1	IO Power 3.3V	
25	XIN24M	I	N/A		XIN24M	Oscillator 24MHz clock input	
26	XOUT24M	O	N/A		XOUT24M	Oscillator 24MHz clock output	
27	EFUSE	P			EFUSE	test write only(2.5v)	
28	GPIO2_B0	I/O	up		Recovery	Low level into Recovery	
29	TEST	I	down		TEST	Enter into test mode,default connect to VSS	
30	GPIO2_C6/UART1_RX	I/O	up		LAN_RST	Ethernet reset output	
31	GPIO2_C7/UART1_TX	I/O	down		HOST_DRV	USB HOST power control output	
32	GPIO1_B0/HDMI_CEC	I/O	up		HDMI_CEC	HDMI_CEC	
33	GPIO1_B3/HDMI_HPD	I/O	down		HDMI_HPD	HDMI Hot Plug Detection input	
34	GPIO1_B2/HDMI_SCL	I/O	up		HDMI_SCL	HDMI I2C serial port,need external pull-up	
35	GPIO1_B1/HDMI_SDA	I/O	up		HDMI_SDA	HDMI I2C serial port,need external pull-up	
36	CVDD2	P			CVDD2	ARM core power supply	
37	USB1_DP	A			USB1_DP	USB HOST1 Data Plus port	

38	USB1_DM	A		USB1_DM	USB HOST1 Data Minus port	
39	USB_AVDD33	AP		USB_AVDD33	USB analog power supply	
40	USB_DVDD11	AP		USB_DVDD11	USB digital power supply	
41	USB_EXTR	A		USB_EXTR	USB reference current generate,connect a 130ohm resistor to VSS.	
42	USB0_VBUS	A		USB0_DET	USB OTG connected detect input	
43	USB0_DM	A		USB0_DM	USB OTG Data Minus port	
44	USB0_DP	A		USB0_DP	USB OTG Data Plus port	
45	HDMI_AVDD33	AP		HDMI_AVDD33	HDMI power supply	
46	HDMI_EXTR	A		HDMI_EXTR	HDMI reference current generate,connect a 1.62K 1% resistor to VSS.	
47	HDMI_VSS	AG		HDMI_VSS	HDMI GND	
48	HDMI_DVDD1V1_1	AP		HDMI_DVDD1V1	HDMI power supply	
49	HDMI_TX3N	A		HDMI_TX3N	HDMI differential pixel clock negative	
50	HDMI_TX3P	A		HDMI_TX3P	HDMI differential pixel clock positive	
51	HDMI_TX0N	A		HDMI_TX0N	HDMI channel 0 differential serial data negative	
52	HDMI_TX0P	A		HDMI_TX0P	HDMI channel 0 differential serial data positive	
53	HDMI_DVDD1V1_2	AP		HDMI_DVDD1V1	HDMI power supply	
54	HDMI_TX1N	A		HDMI_TX1N	HDMI channel 1 differential serial data negative	
55	HDMI_TX1P	A		HDMI_TX1P	HDMI channel 1 differential serial data positive	
56	HDMI_DVDD1V1_3	AP		HDMI_DVDD1V1	HDMI power supply	
57	HDMI_TX2N	A		HDMI_TX2N	HDMI channel 2 differential serial data negative	
58	HDMI_TX2P	A		HDMI_TX2P	HDMI channel 2 differential serial data positive	
59	HDMI_DVDD1V1_4	AP		HDMI_DVDD1V1	HDMI power supply	
60	VDAC_IOUTP	A		VDAC_IOUTP	CVBS OUT	
61	VDAC_AVDD33	AP		VDAC_AVDD33	VDAC power supply	
62	VDAC_IREF	A		VDAC_IREF	VDAC reference current generate,connect a 1K13 1% resistor to VSS.	
63	CODEC_AVSS	AG		CODEC_AVSS	CODEC GND	
64	CODEC_AOR	A		CODEC_AOR	Right channel output	
65	CODEC_AVDD33	AP		CODEC_AVDD33	CODEC power supply	
66	CODEC_VCM	A		CODEC_VCM	CODEC VCM,connect a 4.7uF capacitance to VSS.	
67	CODEC_AOL	A		CODEC_AOL	Left channel output	
68	CVDD3	P		CVDD3	ARM core power supply	
69	GPIO2_C3/MAC_TXD0	I/O	down	MAC_TXD0	MAC transmit data	
70	GPIO2_C2/MAC_TXD1	I/O	down	MAC_TXD1	MAC transmit data	
71	GPIO2_C1/MAC_RXD0	I/O	down	MAC_RXD0	MAC receive data	
72	GPIO2_C0/MAC_RXD1	I/O	down	MAC_RXD1	MAC receive data	
73	GPIO2_D1/MAC_MDC	I/O	down	MAC_MDC	MAC management clock	
74	GPIO2_B7/MAC_RXER	I/O	down	MAC_RXER	MAC receive error	
75	GPIO2_B6/MAC_CLK_IN/MAC_CLK_OUT	I/O	down	MAC_CLK	MAC reference clock output/input	
76	VCCIO2	P		VCCIO2	IO Power 3.3V	
77	GPIO2_B5/MAC_TXEN	I/O	down	MAC_TXEN	MAC transmit enable	
78	GPIO2_B4/MAC_MDIO	I/O	down	MAC_MDIO	MAC management command and data	
79	GPIO2_B2/MAC_CRS	I/O	down	MAC_CRS	MAC carrier sense detect	

80	GPIO0_A1/PWM2/I2C0_SDA	I/O	up		PWM ADJ	ARM Power dynamic voltage scaling control	I2C0_SDA
81	GPIO0_A0/PWM1/I2C0_SCL	I/O	up		BT_HOST_WAKE	BT module wake up CPU	I2C0_SCL
82	GPIO2_C4/I2C2_SDA	I/O	up		WIFI_HOST_WAKE	WIFI module wake up CPU	I2C2_SDA
83	GPIO2_C5/I2C2_SCL	I/O	up		BT_WAKE	CPU wake up BT module	I2C2_SCL
84	GPIO0_D4/SPDIF	I/O	down		SPDIF_TX	SPDIF TX	
85	GPIO0_A2/I2C1_SCL	I/O	up		I2C1_SCL	Serial port 1,need external pull-up	
86	GPIO0_A3/I2C1_SDA	I/O	up		I2C1_SDA	Serial port 1,need external pull-up	
87	CVDD4	P			CVDD4	ARM core power supply	
88	CVDD6	P			CVDD6	ARM core power supply	
89	CVDD7	P			CVDD7	ARM core power supply	
90	GPIO1_D0/FLASH_D0/EMMC_D0/SFC_SIO0	I/O	up		FLASH_D0	Nand Flash/EMMC data port	EMMC_D0
91	GPIO1_D1/FLASH_D1/EMMC_D1/SFC_SIO1	I/O	up		FLASH_D1	Nand Flash/EMMC data port	EMMC_D1
92	GPIO1_D2/FLASH_D2/EMMC_D2/SFC_SIO2	I/O	up		FLASH_D2	Nand Flash/EMMC data port	EMMC_D2
93	GPIO1_D3/FLASH_D3/EMMC_D3/SFC_SIO3	I/O	up		FLASH_D3	Nand Flash/EMMC data port	EMMC_D3
94	GPIO1_D4/FLASH_D4/EMMC_D4/SPI_RXD	I/O	up		FLASH_D4	Nand Flash/EMMC data port	EMMC_D4
95	GPIO1_D5/FLASH_D5/EMMC_D5/SPI_TXD	I/O	up		FLASH_D5	Nand Flash/EMMC data port	EMMC_D5
96	GPIO1_D6/FLASH_D6/EMMC_D6/SPI_CSN0	I/O	up		FLASH_D6	Nand Flash/EMMC data port	EMMC_D6
97	GPIO1_D7/FLASH_D7/EMMC_D7/SPI_CSN1	I/O	up		FLASH_D7	Nand Flash/EMMC data port	EMMC_D7
98	VCCIO3	P			VCCIO3	IO Power 3.3V	
99	GPIO2_A0/FLASH_ALE/SPI_CLK	I/O	down		FLASH_ALE	Nand flash address latch enable	
100	GPIO2_A1/FLASH_CLE/EMMC_CLK	I/O	down		FLASH_CLE	Nand flash command latch enable	EMMC_CLK
101	GPIO2_A2/FLASH_WRN/SFC_CSN0	I/O	up		FLASH_WRN	Nand flash write enable	
102	GPIO2_A3/FLASH_RDN/SFC_CSN1	I/O	up		FLASH_RDN	Nand flash read enable	
103	GPIO2_A4/FLASH_RDY/EMMC_CMD/SFC_CLK	I/O	up		FLASH_RDY	Nand flash read/busy output	EMMC_CMD
104	GPIO2_A6/FLASH_CS0	I/O	up		FLASH_CS0	Nand flash select0 port	
105	CVDD8	P			CVDD8	ARM core power supply	
106	NPOR	I	down		NPOR	System reset input	
107	GPIO1_C5/SDMMC0_D3/JTAG_TMS	I/O	up		SDMMC0_D3	SD/MMC data3 port	JTAG_TMS
108	GPIO1_C4/SDMMC0_D2/JTAG_TCK	I/O	up		SDMMC0_D2	SD/MMC data2 port	JTAG_TCK
109	GPIO1_C3/SDMMC0_D1/UART2_TX	I/O	up		SDMMC0_D1	SD/MMC data1 port	UART2_TX
110	GPIO1_C2/SDMMC0_D0/UART2_RX	I/O	up		SDMMC0_D0	SD/MMC data0 port	UART2_RX
111	GPIO1_C1/SDMMC0_DET	I/O	up		SDMMC0_DET	SD/MMC detect input	
112	GPIO1_C0/SDMMC0_CLKO	I/O	down		SDMMC0_CLKO	SD/MMC clock ouput	
113	GPIO1_B7/SDMMC0_CMD	I/O	up		SDMMC0_CMD	SD/MMC command	
114	VCCIO4	P			VCCIO4	IO Power 3.3V	
115	GPIO0_B6/SDMMC1_D3/I2S1_SCLK	I/O	up		SDMMC1_D3	SDIO1 data3 port, for WIFI module	
116	GPIO0_B5/SDMMC1_D2/I2S1_SDI	I/O	up		SDMMC1_D2	SDIO1 data2 port, for WIFI module	
117	GPIO0_B4/SDMMC1_D1/I2S1_LRCK_TX	I/O	up		SDMMC1_D1	SDIO1 data1 port, for WIFI module	
118	GPIO0_B3/SDMMC1_D0/I2S1_LRCK_RX	I/O	up		SDMMC1_D0	SDIO1 data0 port, for WIFI module	
119	GPIO0_B1/SDMMC1_CLKO/I2S1_MCLK	I/O	up		SDMMC1_CLKO	SDIO1 clock ouput, for WIFI module	
120	GPIO0_B0/SDMMC1_CMD/I2S1_SDO	I/O	up		SDMMC1_CMD	SDIO1 command, for WIFI module	
121	GPIO0_D3/IR	I/O	down		IR_RX	Infrared receiver data input	

122	GPIO0_D2	I/O	down		OTG_DRV	USB OTG power control output	
123	GPIO1_A0/I2S_MCLK	I/O	down		MUTE_CTL	Audio out mute control	I2S_MCLK
124	CVDD9	P			CVDD9	ARM core power supply	
125	GPIO1_A3/I2S_LRCK_TX	I/O	down		WORK/STANDBY_LED	STANDBY LED control	I2S_LRCK_TX
126	GPIO1_A2/I2S_LRCK_RX/PWM0	I/O	down		PCM_SYNC	PCM sync signal	I2S_LRCK_RX
127	GPIO1_A1/I2S_SCLK	I/O	down		PCM_CLK	PCM clock	I2S_SCLK
128	GPIO1_A5/I2S_SDI	I/O	down		PCM_IN	PCM data input	I2S_SDI
129	GPIO1_A4/I2S_SDO0	I/O	down		PCM_OUT	PCM Data output	I2S_SDO0
130	GPIO2_D6/I2S_SDO1	I/O	down		WIFI_REG_ON	WIFI module power enable output	
131	GPIO2_D5/I2S_SDO2	I/O	down		BT_RST	BT module reset output	
132	GPIO2_D4/I2S_SDO3	I/O	down		SDMMC_PWR	SD card power control output	
133	GPIO0_C1/UART0_RX	I/O	up		UART0_RX	UART0 data input, for BT module	
134	GPIO0_C0/UART0_TX	I/O	down		UART0_TX	UART0 data output, for BT module	
135	GPIO0_C3/UART0_CTSN	I/O	up		UART0_CTSN	UART0 clear to send, for BT module	
136	GPIO0_C2/UART0_RTSN	I/O	up		UART0_RTSN	UART0 require to send, for BT module	
137	CVDD11	P			CVDD11	ARM core power supply	
138	DDR_DQ2	A			DDR_DQ2	DDR3 PHY	
139	DDR_DQ0	A			DDR_DQ0	DDR3 PHY	
140	VCC_DDR3	P			VCC_DDR3	DDR3 PHYIO Power 1.5V	
141	DDR_DQS0	A			DDR_DQS0	DDR3 PHY	
142	DDR_DQS0_N	A			DDR_DQS0_N	DDR3 PHY	
143	DDR_DQ6	A			DDR_DQ6	DDR3 PHY	
144	DDR_DQ4	A			DDR_DQ4	DDR3 PHY	
145	DDR_DQ7	A			DDR_DQ7	DDR3 PHY	
146	DDR_DQ5	A			DDR_DQ5	DDR3 PHY	
147	VCC_DDR4	P			VCC_DDR4	DDR3 PHY IO Power 1.5V	
148	DDR_DQ1	A			DDR_DQ1	DDR3 PHY	
149	DDR_DM0	A			DDR_DM0	DDR3 PHY	
150	DDR_DQ3	A			DDR_DQ3	DDR3 PHY	
151	VCC_DDR5	P			VCC_DDR5	DDR3 PHY IO Power 1.5V	
152	DDR_A8	A			DDR_A8	DDR3 PHY	
153	DDR_A6	A			DDR_A6	DDR3 PHY	
154	DDR_A14	A			DDR_A14	DDR3 PHY	
155	DDR_A15	A			DDR_A15	DDR3 PHY	
156	DDR_A11	A			DDR_A11	DDR3 PHY	
157	DDR_A1	A			DDR_A1	DDR3 PHY	
158	DDR_A4	A			DDR_A4	DDR3 PHY	
159	DDR_A12	A			DDR_A12	DDR3 PHY	
160	CVDD10	P			CVDD10	DDR3 PHY CORE Power	
161	DDR_BA1	A			DDR_BA1	DDR3 PHY	
162	DDR_BA0	A			DDR_BA0	DDR3 PHY	
163	DDR_A10	A			DDR_A10	DDR3 PHY	

164	DDR_CKE	A			DDR_CKE	DDR3 PHY	
165	DDR_ODT0	A			DDR_ODT0	DDR3 PHY	
166	DDR_CLK_N	A			DDR_CLK_N	DDR3 PHY	
167	DDR_CLK	A			DDR_CLK	DDR3 PHY	
168	VCC_DDR6	P			VCC_DDR6	DDR3 PHY IO Power 1.5V	
169	DDR_RASN	A			DDR_RASN	DDR3 PHY	
170	DDR_CASN	A			DDR_CASN	DDR3 PHY	
171	DDR_CSN1	A			DDR_CSN1	DDR3 PHY	
172	DDR_CSN0	A			DDR_CSN0	DDR3 PHY	
173	DDR_WEN	A			DDR_WEN	DDR3 PHY	
174	DDR_BA2	A			DDR_BA2	DDR3 PHY	
175	DDR_A3	A			DDR_A3	DDR3 PHY	
176	VCC_DDR7	P			VCC_DDR7	DDR3 PHY IO Power 1.5V	
ePAD	ePAD	G			ePAD	ePAD	